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Behavioural Models for Analog to Digital Conversion Multi-steps Architectures

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ABSTRACT

Multi-stage analog-to-digital converters are the dominant choice in applications that require both high speed and high accuracy, such as video and wideband radio [1]. Non-idealities such as static device mismatch and dynamic timing mismatch, in different architectures of multi-steps analog to digital converter affect the redundancy and performance at the output of an instrument. Redundant sign digit (RSD) is an approach of calibration have been proposed to detect and automation no anymore only for cyclic converter but also for multistage A/D with M-bits per cycle for correction of errors in order to improve the resolution and the redundancy of A/D converters and to adapt the high performance of digital signal processing system. In this paper we will presented a behavioral model in order to investigate the impact of different sources of error at different levels of simulation based at the comparison of RSD to conventional converter with Z extra decision level (CRZ). As result, the RSD converter show a performance equivalent to CRZ with $Z=2^M -1$ where M is the number of bits per cycle.

Keywords: *A/D converters, CRZ architecture, RSD architecture,Matlab simulation.*

1. INTRODUCTION

The relevance of data converters for mixed analog-digital systems urges the availability of fast, reliable and accurate simulation tools. They are necessary to validate algorithms or architectures and must employed to evaluate static and dynamic responses of the ADCs or DACs [2].

Different approaches of calibration have been proposed to detect and automation correction of errors in order to improve the resolution and the redundancy of A/D converters and to adapt the high performance of digital signal processing system (DSP) [3], [4]. Two main possibilities to introduce redundancy to multi-steps converters in such:

a. Adding a number of extra decision levels in the flash used at each step.
b. Using a different coding strategy (Redundant Signed Digit, RSD) based on three instead of two state digits.

In this work to investigate the tolerance behavior of two step 10 bits converter by using the Matlab by using two different approaches, the behavioral model to best understand the function of multi-step converter and the circuital model for real design with the exciting CMOS technology, more than 10 bits of resolution it becomes extremely time-consuming exploring all the codes. Even with a powerful computer, the simulation time becomes so long that designer utilizes transistor-level analysis only for studying critical transition points: it assumes that if the circuit operates properly in the critical (or presupposed to be critical) points, it will work satisfactorily for any condition of operation. The strategy is obviously risky and it should be, at list, complemented by a less particularized but exhaustive system analysis.

2. MULTI STAGE ANALOG TO DIGITAL CONVERTER

The classical architecture of n-stages converters are presented in Fig.1: M=N/n bits are produced each time a new cycle is launched, starting from the MSB until the LSB, N being the resolution of the converter. Started the conversion from the coarse one by calculate the difference between the input and the analog counterpart of the digital word produced at the end of the first cycle, the residue (Ri) produced at the end of each cycle will be the input of the followed conversion that will be more fine then precedent conversion. In this way, we will use the same hardware in each cycle.

Different sources of error in reality affect the conversion in each cycle, transition position errors produced at A/D flash converter, transition magnitude errors produced by parallel D/A converter, also relative gain error of the multiply by 2^M function and finally the offset error of the OpAmp.

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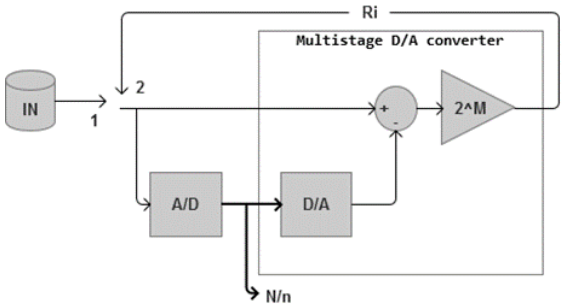

Fig 1: RSD cyclic conversion algorithm

3. THE CONVENTIONAL RESTORING CONVERTERS WITH Z ADDITIONAL LEVELS

The CRZ converters consisting of converter obtained from the conventional CR adding Z additional levels, in order to reduce the sensitivity against transition position errors by automatic correction that occurs while cycling. The concept of this converter explained by Robertson plot, a graphical tool that illustrates the way residue calculation perform used to interprets the cyclic algorithm. The algorithm to calculate Ri's remainders or residues [5]:

$$R_{i+1} = 2^{i}.\{R_1 - \sum_{j=1}^{i}(b_j.2^{-j}).V_{ref}\}$$

With bj = - 1 or 1, and R1= Vin

$$\lim_{i\to\infty}\sum_{j=1}^{i}(b_j.2^{-i}) = \frac{V_{in}}{V_{ref}}$$

$$R_1 = 2^2 * (V_{in} - 3 * \frac{1}{2^2})$$

Fig.2 is an example of ideal 3-steps, 6 bits converter to convert VIN = +0.57. The first step, the input signal is reported along the Y-direction until it reaches the line D = (1 1 1); the point of intersection implements the first remainderR_1, giving the input for the second step which must be now reported along the X-direction until it reaches the lineD = (-1 -1 -1). The procedure repeated in this way until the least significant bits are produce.

In real, errors will be affecting the conversion in each cycle and the correctness of the conversion process, because residues will be not necessary stay inside the region bounded by the dashed square. Fig .3 showing for Vin but 5%. Due to this error, the signature departs progressively from the ideal as the cycle count increases: error on transition position the trajectory leaves the conversion region and the converter saturates after R1.

To reduce of the sensitivity of the converter some additional levels are introduce and that allowed defining a larger convergence region in order to improve the redundancy of converter. In fig.4 a two additional level are introduce to the previous case called Z levels. Owing to the dynamic range of residues, which is bound in practice by the power supply, it is necessary to consider a scale factor K that multiplies both the reference scale of the flash converter and the unit elements of the D to A parallel converter:

$$K = \frac{2^M - 1}{2^M - 1 + Z} \qquad (1)$$

Where M is the number of bits produced at each cycle. Now, even in presence of some errors, the trajectory stays inside the convergence region. However, the larger strength of CRZ converters against transition position error paid in terms of area and power consumption: where the number of comparators will increase Z comparators to detect the position of the input signal.

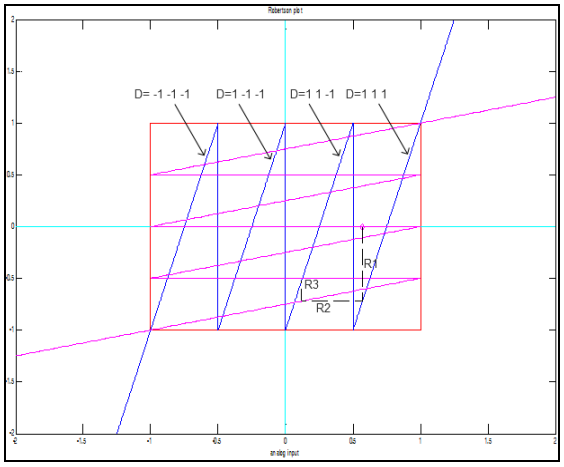

Fig 2: Robertson plots of a 6-bit, 3-cycles conventional CR converter ideal case

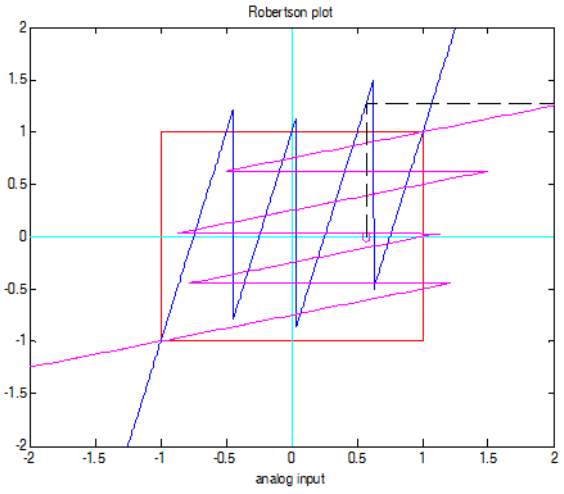

Fig 3: Robertson plots of a 6-bit, 3-cycles conventional CR converter real case

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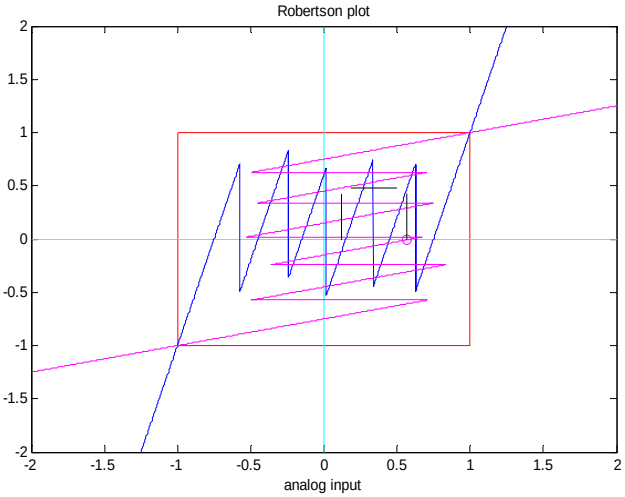

Fig 4: Robertson plots of a 6-bit, 3-cycles conventional CR converter, Z=2

4. RSD ALGORITHM

The RSD (Redundant Signed Digit) used with new architecture by [6]as showed in Fig.3, to overcome the offset errors in the conventional Cyclic ADC, and to facilitate high-resolution conversion without having to use accurate voltage comparators. The analog input is compared simultaneously with two thresholds (P and Q) and a single RSD digit is produced [3,4,5], the selection signal is now also allowed to be equal to 0, and the decision rule changes following the Robertson diagram represent in Fig.5, will Fig.6 represent the Robertson diagram.

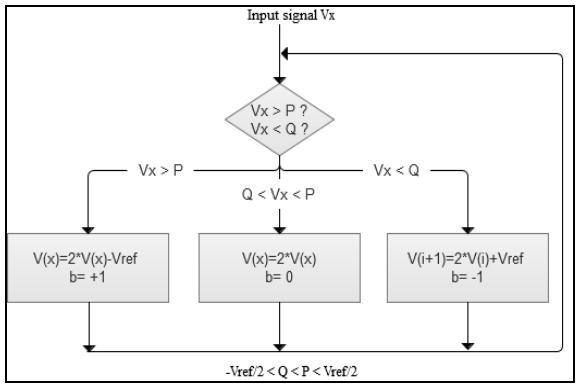

Fig 5: RSD cyclic conversion algorithm.

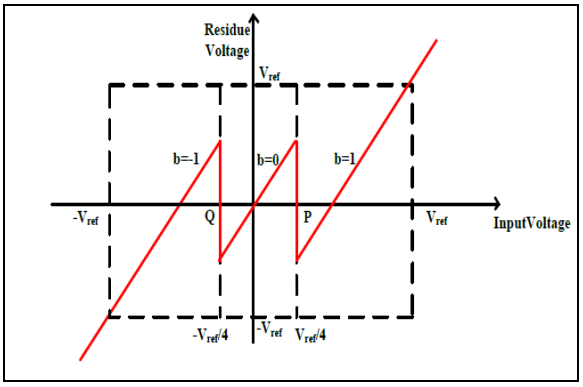

Fig 6: Residue Plot of a 1.5-bit/stage Architecture

5. RELATION BETWEEN CRZ AND RSD

While the number of comparators needed, in case of CRZ, to detect the position of the input signal are (2^M+1+Z) comparators respect to the thresholds defined by resistors of the (2^M-1) reference divider. The RSD mythology produce a double threshold concept underlying the redundant single-bit converter as explain before, that mean a $2*(2^M-1)$ comparators are needed to detect the position of the analog input with respect to the thresholds defined by (2^M-1) resistors of the reference divider.

For $Z = 2^M - 1$ the CRZ and RSD flash reference are identical meaning that the impact of transition position errors is the same for both converters, because the transition positions and the number of comparators and resistors of the reference divider are the same. However, because of the different coding algorithms, the D to A parallel converters differs. In particular, since the input signal is compared simultaneously with two thresholds to produce a single RSD digit, the output thermometric code from the RSD converter requires half the digits of the equivalent CRZ converter. As a result, the number and the magnitude of unit elements required by the D to A parallel converter are different. Table 1 compares the characteristics of the two converters in terms of the number of components [with K defined by (1)].

Table 1: Comparison between CRZ and RSD

	Comparators	Resistors	ue (h)	ue size
CRZ	(2^M-1+Z)	(2^M+Z)	(2^M-1+Z)	$\frac{1}{2^M}\times K$
RSD	$2*(2^M-1)$	$(2^{M+1}-1)$	(2^M-1)	$\frac{1}{2^M}$

6. BEHAVIOURAL MODEL

Due to the increasing complexity of circuits and systems the using a behavioral models suitable for both CRZ and RSD converters, helps in achieving the target, and it is useful to understand how a real converter behaves when non-idealities such transition position and transition magnitude errors appears without considering circuit design aspects. Behavioral simulators work much faster than the transistor level counter parts thus permitting to

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explore all the regions of operation. The proposal Behavioral Simulator of multi-stage analog to digital converter consists of three main parts: input data consist of input signal, the parameters, and voltage references and OpAmp gain, the simulation blocks that contain analog to digital flash converter and parallel digital to analog converter, finally the output consist of database SNR as showed in Fig.5. Where each block is modulated by a corresponding matlab function. The bold lines indicated a digital output.

For two cycles analog to digital converter, the input signal Vin, read from a data base containing the sampled pure sine wave, is applied to the flash converter (1).

The flash references are introduced the impairments on transition positions of A/D by means of the parameter σ_{comp} included in flash reference, which portrays the standard deviation of a standard distribution with zero mean value. The thermometric code delivered by the flash converter is temporarily stored in a register (coarse conversion) before being sent to a parallel D/A converter.

The impairments on the D/A conversion are introduced through unit element by the parameter σ_{ue}: unit elements differ from the ideal value by an error which is described also by means of a standard distribution with zero mean value and standard deviation σ_{ue}.

The residue, computed as the difference between the input signal VIN and the analog counterpart of the coarse conversion, is amplified before being recycled for the fine conversion (2).
Finally, the gain error of the amplifier is set by the parameter relGain.

7. EFFECT OF DIFFERENT SOURCES OF ERRORS

The Malatb program is used to modulate the different block that showed in fig.7. The simulation is 2 cycles 10 bits A/D. The resultants produced such as ENOB, Nfs and fast Fourier transform (Fft) that measures the entire data acquisition system from the signal input to the resulting data values, would be useful later to make decision in the circuit design.

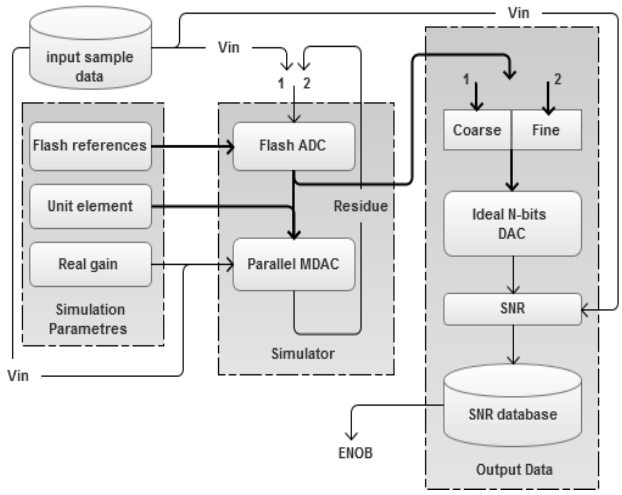

Fig 7: Block diagram of Behavioral Simulator

7.1 Effect of transition Position Errors

The results of the analysis concerning the impact of transition position errors on CRZ converters are presented in fig.8, While the ENOB remains above 10-bit whichever Z and $\boldsymbol{\sigma_{comp}}$, the Nfs drops dramatically when few additional levels are considered as represented in fig.8. The dashed black lines on both curves portray the locus of larger$\boldsymbol{\sigma_{comp}}$ lead to references overlapping, and errors cannot be corrected anymore.

The spectral signatures for several CRZ converters with respect to different values of$\boldsymbol{\sigma_{comp}}$, $\boldsymbol{\sigma_{comp}}$=0.003 in fig.9 and$\boldsymbol{\sigma_{comp}}$=0.01 in fig.10. The impact of transition position errors drops at the output response with larger Z as derived from the analysis of the SNR loci, thanks to the automatic correction occurring in the fine conversion. Notice that transition position errors do not introduce any spurious frequency in the output spectra.

7.2 Effect of Transition Magnitude Errors

When small input signals are considered, the ENOB is not affected by transition magnitude errors because The CRZ converters with odd Zs are less sensitive against transition magnitude errors However, the ENOB is more enhancement with the number of additional levels, and for $Z=2^M-1$ the accuracy of the converter is one-bit larger as showed in fig.11. With lager input signal, the impact of transition position errors becomes more clear as shown by the N_{fs}, which drops for larger $\boldsymbol{\sigma_{ue}}$. As for transition position errors, again, the dashed lines portray the locus of $\boldsymbol{\sigma_{ue}}$, where larger$\boldsymbol{\sigma_{ue}}$ lead to non-monotoni city errors.

The fft test shows that transition magnitude errors add some spurious frequencies, which are well above the noise floor in the spectra of the considered CRZ converters. In Fig.12 is reported two cases with σue = 0.003 and $\boldsymbol{\sigma_{ue}}$ = 0.01. Notice that transition position errors do not introduce any spurious frequency in the output spectra

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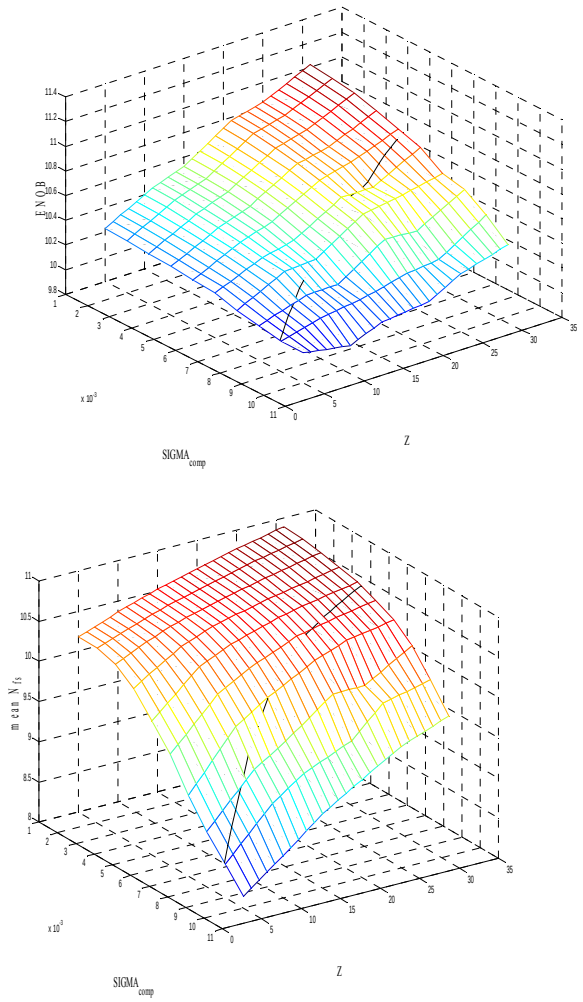

Fig 8: Impact of transition position errors on CRZ converters.

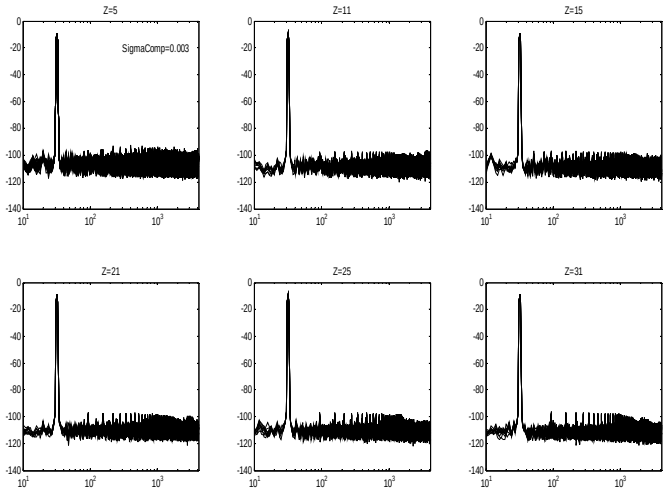

Fig 9: Spectral signature for σ_{comp}=0.003.

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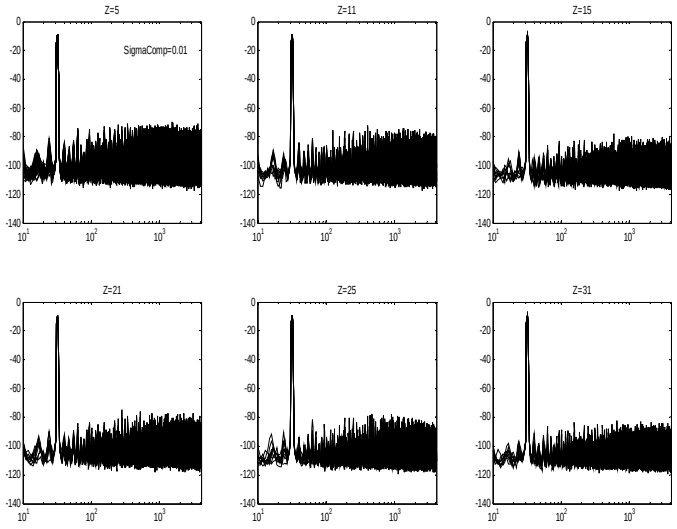

Fig 10: Spectral signature for σ_{comp}=0.01.

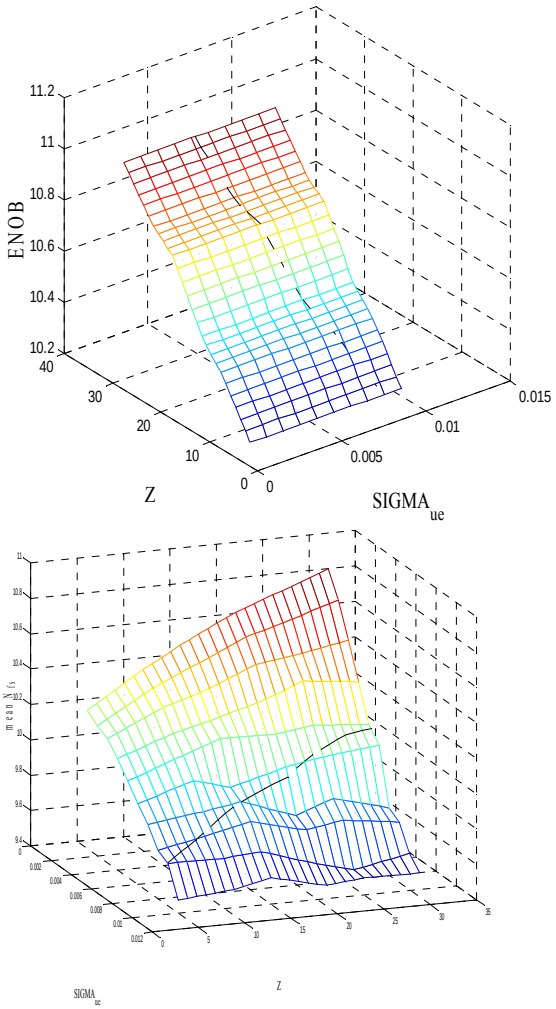

Fig 11: Impact of transition magnitude errors on CRZ converters.

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7.3 Effect of the Gain Error

The effect of gain error will be clearer effect the response of multi-step analog to digital converter if few bits are produced each cycle, as showed the simulation in fig.13. With the same additional level Z but with at two different levels of real gain = 1.01 and 1.1 the N_{fs} is case of 1.01 is highest by 1.7 bits approximately than 1.1. In addition, the number of cycle

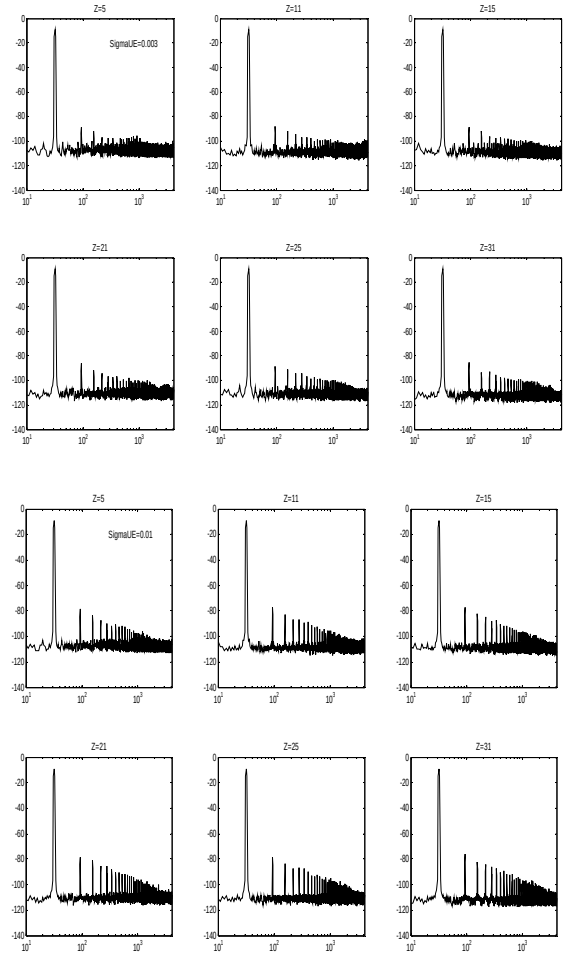

Fig 12: Spectral signature for σ_{ue} =0.003 and σ_{ue} =0.01.

8. CONCLUSION

The behavioral model introduced in the previous is a good intuitive model, useful to understand how a real converter behaves when non-idealities such transition position, transition magnitude and gain errors appears, and allow us to make a comparison between two menologies of redundancy. The effect of different sources of error at the performance and the resolution of ADC converter are estimated, but it is not enough for design. Specially the model in not interconnect or interactive with real parameters and not include the non-idealities related to devices mismatch issues, a circuital design is mandatory to verifying all previous results.

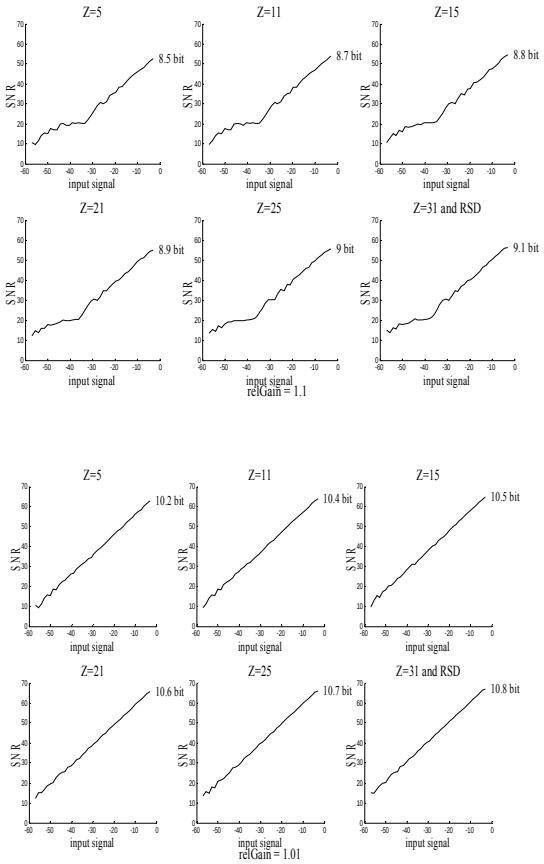

Fig 13: Impact of real gain error at the Nfs.

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