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# Efficient Implementation of Carry Free Select Adder

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## ABSTRACT

Datapath logic is a most important element in VLSI system design. The design of datapath logic requires more attention to develop efficient application. This paper presents carry free select adder for datapath logic. This paper evaluates and implemented the carry free select adder using Verilog HDL and the performance has been analyzed completely in terms of Area, Power, and Delay by targeting to 0.18um CMOS process technology the proposed design processed on RTL Compiler and SoC encounter. The results shown optimized hardware and speed efficient carry select adder.

**Keywords:** *Data path logic, Carry Select Adder, Carry Free Adder.*

## 1. INTRODUCTION

VLSI system design flow comprises different level, in that the Register transfer level is one of the lower levels. The RTL level shows the dataflow model of the design which describes register level transfer activity i.e., sequence in which the register transfer action takes place and it is decided by the control signals and the activity refers to moving of the data around some specified path. To have various components together and based upon the processor requirement, the controller will issue the control signals so that the physical connections are enabled and the data will be move around the path.

In ASIC design, cell-based design techniques, for instance data path design and FPGA's together with flexible hardware synthesis are the bare bones for a high productivity. Addition, multiplication and accumulation are the foremost decisive operations of digital signal processing (DSP). In DSP or control system, addition is a requisite operation for any digital system. Therefore, the recital of the resident adders is greatly influenced by fast and accurate operation of a digital system. An adder plays a prominent role in digital systems due to their rife usage in other basic digital operations for example subtraction, multiplication and division [1]. In last decade scores of adder architectures have been premeditated and proposed for hastening of the binary operations. Concern with circuit area, speed as well as aptness for logical optimization and synthesis, the data path adders are well characterized. The simplest adder is ripple carry adder [2,3], but having slowest performance with both area and delay of n orders, it linearly increases with size of bits. Usually Carry Look-Ahead adder [4] suffers from lopsided layout with both area and delay of Order of logarithmic value of n. Further adders like Carry Skip Adder (CSA) [5,6], Carry Increment [7] and Carry Select Adder (CSLA)[8] provides a good negotiation in terms of area and delay. The above mentioned adders have an area of Order of n and delay of Order of $n^{t+2/l+1}$ and provides a trouble-free and customary layout. Carry Save Adder has an area of Order of n and delay of Order of multiplication of n and logarithmic value of n. By providing no limit on fan in/out the Carry Look-Ahead adders have been realized in two gate levels. By the process of pre-computation, the sum of all possible carry bit values (i.e. '0' and '1') the Carry Select Adder (CSLA) will trim down the computation time. After the available of carry, the appropriate sum has been selected using multiplexer. In the classification of fast adders the carry select adder plays a prominent role, but it suffers from limitation of fan-out because the numbers of multiplexers which are needed to be driven by the signal of carry rapidly increases [1].

The following sections explains the carry free adder, the proposed design of 16-bit carry free select adder & it's working and detail explanation of implementing the 16-bit adder on TSMC 0.18 technology, their gate level schematic and layout view.

## 2. CARRY FREE ADDER

In most of the adder designs carry propagation plays a vital role by which the delay increases rapidly and slow down the speed of operation so that we move on to carry free adder to decrease the delay and increase the speed of operation. Carry free can be achieved by redundant number system [9]. The important property of this is to have more than one representation for its value and to represent negative number easily. This representation limits the carry propagation to a few bits, which is usually independent of the word length W. The carry free adder circuit internally consists of interm sum and interm transfer digit. The final sum can be achieved with carry free property is by shifting the interm transfer digit one position to left and adding the interm sum bits to it.

## 3. PROPOSED DESIGN

As mentioned in previous section, the carry became the critical path for any datapath logic. This can be eliminated by using the carry free adder. Fig1 shows the 4-bit CFSL adder having A and B as input which results SUM of 5-bit. This is the modified structure of carry select adder. The regular carry select adder [10] contains the Ripple carry adder, which performance became sensitive to length of input. For higher length, the performance gets degraded. So this paper introduces the redundant arithmetic on carry select structure which performs better in Area and delay.

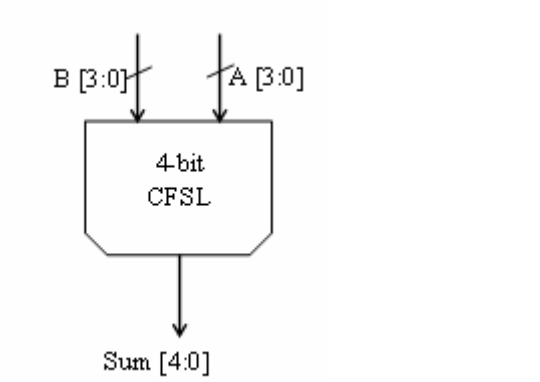


**Fig 1:** 4-bit Carry free select adder

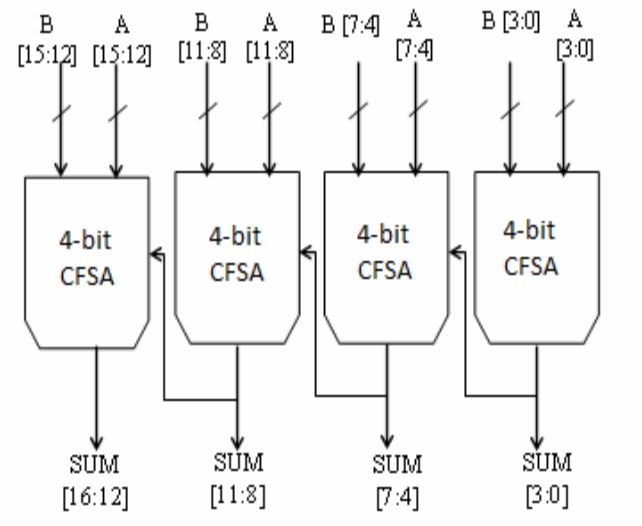


**Fig 2:** Chain of 4-bit carry free select adder (16-bit adder)

This paper works on 16-bit adder which shown in Fig 2. A, B, and SUM, are the output variables respectively. This structure is very simple and looks like ripple carry structure. So that the delay of each block is similar and less because of free from carry propagation [10]. Instead propagating the carry here we considering MSB as carry for each 4-bit carry free select adder.

## 4. IMPLEMENTATION AND RESULT

The above design targeted for ASIC, 0.18 cmos processing technology. The design can represent in Verilog HDL code and undergone functional simulation using modelsim 6.3f. The simulated outputs are verified with manual calculation and various structure of carry select adder. The functionally verified design is given as input to the RTL compiler. For running the rtl complier the script file is prepared using tcl script. The tcl script contains the Verilog coding of design and targeted technology library file which can be read using command of “read_hdl”.

Then the design has been elaborated and mapped. The gate level netlist is stored in same Verilog format and verified the design with same set of inputs.

The schematic view of gate level netlist is shown Fig3.

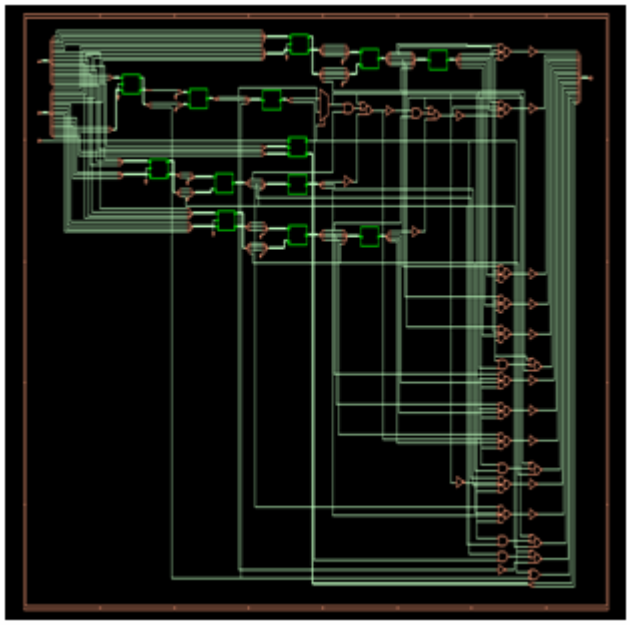

**Fig 3:** Schematic view of gate level netlist

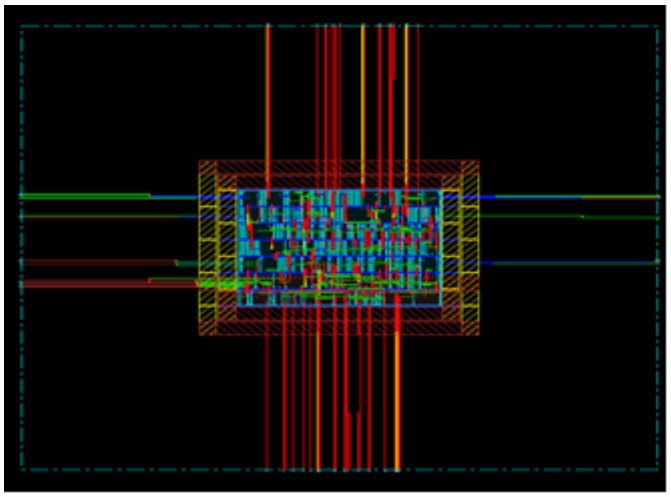

**Fig 4:** Lavout view of 16-bit

After successful completion of gate level simulation, the netlist file is provided to SoC encounter along with the other technology files. Finally the layout has been generated by SoC encounter which shows in the figure Fig4.

**Table 1:** Summarize report of result in terms of area, delay and power

| Proposed design | Transistor count | Delay ns) | Internal power (mW) | Switching power (mW) | Leakage power W) |
|---|---|---|---|---|---|
| 16-bit CFSLA | 191 | 1.925 | 0.2091 | 0.2442 | 8.826 |

Table 1 summarize the performance of area, delay and power for the targeted technology file, the power supply vdd used is 1.8v which itself describes low power structure. From the above table the leakage power is very less of nano watt hence; it may become more reliable of datapath logic for low power application.

## 5. CONCLUSION

A simple approach is proposed in the existing carry select adder to increase the performance mainly in terms of Area. The 16-bit CFSLA has been verified and implemented; the rtl view and layout view are studied. The overall report summary is given in Table1, which shows the effectiveness of design. This paper also shows importance over adder in datapath logic and VLSI system design.

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